

Product Preview

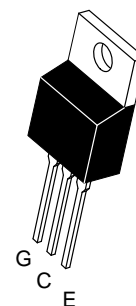
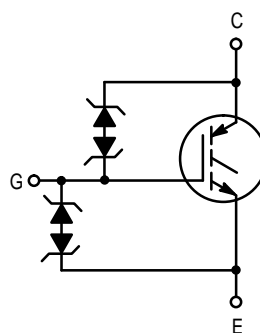
Internally Clamped N-Channel IGBT

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate Collector Over–Voltage Protection from monolithic circuitry for usage as an Ignition Coil Driver.

- Temperature Compensated Gate – Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability

MGP15N43CL

**15 AMPERES
N–CHANNEL IGBT
V_{CE(on)} = 1.8 V
430 VOLTS
CLAMPED**



**CASE 221A–09
STYLE 9
TO–220AB**

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CES}	CLAMPED	V _{dc}
Collector–Gate Voltage	V _{CER}	CLAMPED	V _{dc}
Gate–Emitter Voltage	V _{GE}	CLAMPED	V _{dc}
Collector Current — Continuous	I _C	15	A _{dc}
Total Power Dissipation Derate above 25°C	P _D	136 0.91	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to 175	°C

UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Collector–to–Emitter Avalanche Energy	E _{AS}		mJ
V _{CC} = 50 V, V _{GE} = 5.0 V, PEAK I _L = 14.2 A, L = 3.0 mH, Starting T _J = 25°C		300	
V _{CC} = 50 V, V _{GE} = 5.0 V, PEAK I _L = 10 A, L = 3.0 mH, Starting T _J = 150°C		150	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Case — Junction–to–Ambient	R _{θJC} R _{θJA}	1.1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MGP15N43CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Clamp Voltage (I _C = 1.0 mA, T _J = –40°C to 175°C)	V _{(BR)CES}	—	430	—	Vdc
Zero Gate Voltage Collector Current (V _{CE} = 360 V, V _{GE} = 0 V) (V _{CE} = 360 V, V _{GE} = 0 V, T _J = 150°C)	I _{CES}	— —	— —	10 150	μA _{dc}
Gate–Emitter Clamp Voltage (I _G = 5.0 mA)	V _{(BR)GES}	17	—	22	Vdc
Gate–Emitter Leakage Current (V _{GE} = 10 V)	I _{GES}	—	—	10	μA _{dc}

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{GE} = V _{CE} , I _C = 1.0 mA) Threshold Temperature Coefficient (Negative)	V _{GE(th)}	1.3 —	1.8 4.4	2.1 —	Vdc mV/°C
Collector–to–Emitter On–Voltage (V _{GE} = 3.5 V, I _C = 6.0 A) (V _{GE} = 4.0 V, I _C = 10 A, T _J = 150°C)	V _{CE(on)}	— —	— —	2.0 1.8	Volts
Forward Transconductance (V _{CE} = 5.0 V, I _C = 10 A)	g _{fe}	8.0	20	—	Mhos

DYNAMIC CHARACTERISTICS

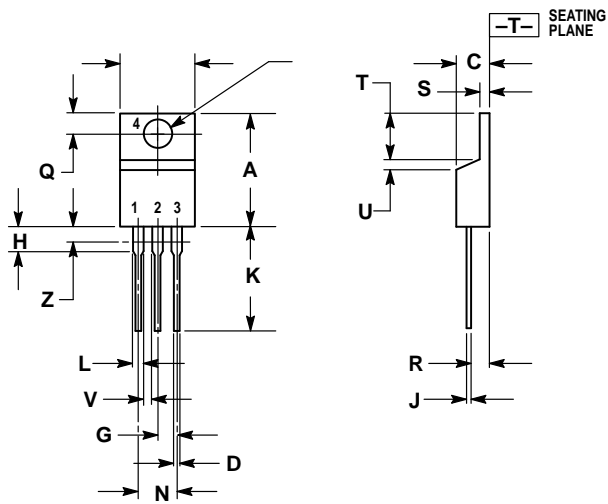
Input Capacitance	(V _{CC} = 15 V, V _{GE} = 0 V, f = 1.0 MHz)	C _{ies}	—	TBD	—	pF
Output Capacitance		C _{oes}	—	TBD	—	
Transfer Capacitance		C _{res}	—	TBD	—	

SWITCHING CHARACTERISTICS (1)

Turn–Off Delay Time	(V _{CC} = 400 V, I _C = 6.5 A, R _G = 1.0 kΩ, L = 300 μH)	t _{d(off)}	—	TBD	—	μSec
Fall Time		t _f	—	TBD	—	
Turn–On Delay Time	(V _{CC} = 10 V, I _C = 6.5 A, R _G = 1.0 kΩ, R _L = 1.0 Ω)	t _{d(on)}	—	TBD	—	μSec
Rise Time		t _r	—	TBD	—	
Gate Charge	(V _{CC} = 350 V, I _C = 15 A, V _{GE} = 5.0 V)	Q _T	—	TBD	—	nC
		Q ₁	—	TBD	—	
		Q ₂	—	TBD	—	

(1) Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS




STYLE 9:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-09
 ISSUE Z

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